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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,033	02/27/2004	Michael Bauer	I431.103.101/FIN 423 US	8344

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EXAMINER	
SEFER, AHMED N	
ART UNIT	PAPER NUMBER
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/789,033	BAUER ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-14 and 18-20* is/are pending in the application.

4a) Of the above claim(s) *18-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed October 2, 2006 has been entered and new claims 18-20 have been added.

Election/Restrictions

2. Newly submitted claims 18-20 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: The semiconductor assembly comprising, inter alia, an insulating circuit substrate comprising lines running parallel on its top side providing a bus line as recited is patentably distinct from the semiconductor wafer comprising integrated circuits arranged in rows and columns on the wafers top side.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 18-20 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, **the plurality of additional semiconductor wafers recited in claim 4** and the semiconductor wafers ... perpendicular **a top side of the substrate recited in claim 6** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The recitation of claim 6 calling for, "... perpendicular a top side of the substrate" should read, "... perpendicular a top side of the **insulated** substrate."

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claim 4 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The application as originally filed does not specifically support the claim limitation "a plurality of additional semiconductor wafers ..." The specification merely discloses a single semiconductor wafer 1 (fig. 3).

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 4 and 6-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 recites the limitation "the plurality of semiconductor wafers chips." There is insufficient antecedent basis for this limitation in the claim.

Claim 6 recites the limitation "the semiconductor wafers." There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

10. Claim 4, as understood, is rejected under 35 U.S.C. 102(b) as being anticipated by Nelson ("Nelson") USPN 4,930,216 (of record).

Nelson discloses figs. 1 and 4-11 a semiconductor wafer (col. 3, lines 35-44) with a top side and a rear side, the semiconductor wafer comprising integrated circuits for semiconductor chips 12 arranged in rows and columns on its wafer top side; strip-type separating regions (col. 3, lines 52-58) arranged between the integrated circuits of the semiconductor chips; wherein the separating regions have passage contacts 30/36 in the direction of the rear side of the semiconductor wafer, the passage contacts having perforations (fig. 10) with walls having a metal layer 34 applied thereto; wherein the walls have also an insulation layer 32 applied thereto; wherein a plurality of additional semiconductor wafers (figs. 6-8) are provided and oriented such that the rear side of the semiconductor wafers are virtually perpendicular to a top side of a circuit substrate 42 (fig. 11) and such that the passage contacts 36 are arranged on the top side of the circuit substrate and up so that the plurality of semiconductor wafers chips are connected (col. 3, lines 36-50) in parallel.

11. Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by Nakajima ("Nakajima") JP 2002-299372 (of record).

Nakajima discloses figs. 1-6 a semiconductor wafer 2 with a top side and a rear side, the semiconductor wafer comprising integrated circuits for semiconductor chips 20 arranged in rows and columns on its wafer top side; strip-type separating regions **DL** arranged between the integrated circuits of the semiconductor chips; wherein the separating regions have passage

contacts 6/10 in the direction of the rear side of the semiconductor wafer; wherein the passage contacts have fusible solder material 31 (e.g. nickel/gold, see fig. 6 and page 4, par. 2.1 of machine translated document); wherein the semiconductor wafer is provided and oriented such the rear side of the semiconductor wafer is virtually perpendicular to a top side of a circuit substrate (figs. 4, 5 and 9) and such that the passage contact are arranged on the top side of the circuit substrate.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 6-14, as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima in view of Koike et al. ("Koike") WO 03/012868.

Nakajima discloses figs. 1-6 a semiconductor chip 20 with a top side, a rear side, and with edge sides (fig. 4), the semiconductor chip comprising an integrated circuit 1 on the top side; at least one edge side having edge contacts 3/6 wherein, the edge contacts extend from the top side in the direction of the rear side of the semiconductor chip; wherein the edge contacts are connected to electrodes of the integrated circuit via conductor tracks (fig. 2) located on the top surface of the semiconductor chip, but lacks anticipation of additional chips stacked one on the other.

Koike discloses figs. 6, 23 and 32 (see also equivalent reference USPN 7,071,028) a plurality of semiconductor chip 3 stacked one on the other and are electrically connected via edge contacts 4/9 among one another and also with respect to external contacts 7/8 on an insulated substrate 18 such that the rear sides of the semiconductor wafers are oriented virtually perpendicular a top side of the substrate.

Regarding claims 7 and 8, Nakajima discloses edge sides having a perforation-like structure, semicylinder-like cutouts extending as edge contacts from the top side in the direction of the rear side (figs. 2 and 4), and having a metal layer 6 (fig. 3) or an insulating layer 5 (as in claim 8).

Therefore, in view of Koike's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Nakajima's device by incorporating additional chips stacked one on the other so as to increase capacity as taught by Koike.

Regarding claim 9, Nakajima discloses cutouts having a soldering material 31(e.g. nickel/gold, see page 4, par. 2.1 of machine translated document).

Regarding claim 10, Nakajima discloses edge contacts being extended on the top side to form a contact area 3 and merge with a conductor track (fig. 2) on the top side.

Regarding claim 11, Nakajima discloses a semiconductor chip being arranged on a circuit substrate (figs. 5 and 12) within an electronic component (fig. 1).

Regarding claims 12 and 14, Nakajima discloses in fig. 12 a circuit substrate (region under layer 12) having a conductor track structure 71, the semiconductor chip 20 being arranged with its rear side on the top side of the circuit substrate or with an edge side on the circuit substrate, the top side of the chip being arranged in angular (figs. 9-12) fashion wrt the top side

of the substrate (as in claim 14) and the edge contacts (fig. 2 and 4) being electrically connected to the conductor structure via contact pads 72 on the top side of the circuit substrate.

Regarding claim 13, Koike discloses the employment of an insulating plastics 5 arranged on a circuit substrate in a manner embedding edge sides of the chip and contact pads 4.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
December 22, 2006

LEONARDO ANDUJAR
PRIMARY EXAMINER